

PST KP1250-20

HIGH POWER PHASE CONTROL THYRISTOR FOR PHASE CONTROL APPLICATIONS

Features :

- Blocking Capability up to 2000 V
- High dV/dt Capability
- All Diffused Structure
- Amplifying Gate Configuration
- Rugged Ceramic Hermetic Package

ELECTRICAL CHARACTERISTICS AND RATINGS

Blocking

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Repetitive peak reverse voltage	V_{RRM}		2000		V	$T_j = -40\text{ °C to }125\text{ °C}$
Repetitive peak off-state voltage	V_{DRM}		2000		V	$T_j = -40\text{ °C to }125\text{ °C}$
Non repetitive peak reverse voltage	V_{RSM}		2100		V	$T_j = -40\text{ °C to }125\text{ °C}$
Repetitive peak reverse current	I_{RRM}		100		mA	$T_j = T_{jmax}, V = V_{RRM}$
Repetitive peak off-state current	I_{DRM}		100		mA	$T_j = T_{jmax}, V = V_{DRM}$

Conducting

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Average value of on-state current	$I_{T(AV)}$		1250		A	50 Hz sine wave, 180° conduction, $T_c = 90\text{ °C}$
RMS value of on-state current	$I_{T(RMS)}$		1963		A	50 Hz sine wave, 180° conduction, $T_c = 90\text{ °C}$
Surge non repetitive current	I_{TSM}		28		kA	50 Hz (10 ms) sine wave Half cycle, $T_j = 25\text{ °C}$
Surge non repetitive current	I_{TSM}		24.5		kA	50 Hz (10 ms) sine wave Half cycle
I square t	$I^2 t$		3000		kA^2s	$V_R = 0$ $T_j = T_{jmax}$
Surge non repetitive current	I_{TSM}		17		kA	50 Hz (100 ms) sine wave Half cycle, $T_j = T_{jmax}$
Peak on-state voltage	V_{TM}		1.75		V	On-state current 4000 A, $T_j = T_{jmax}$
Threshold voltage	$V_{T(TO)}$		0.95		V	$T_j = T_{jmax}$
On-state slope resistance	r_T		0.200		mΩ	$T_j = T_{jmax}$
Holding current	I_H			300	mA	$V_D = 12\text{ V}; I_T = 2.5\text{ A}$
Latching current	I_L			1500	mA	$V_D = 12\text{ V}; R_L = 12\text{ Ω}$

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Triggering

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Gate current	I_{GT}		300		mA	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = -40\ ^\circ\text{C}$
			150		mA	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = 25\ ^\circ\text{C}$
			125		mA	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = 125\ ^\circ\text{C}$
Gate voltage	V_{GT}		5		V	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = -40\ ^\circ\text{C}$
			3		V	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = 0 \div 125\ ^\circ\text{C}$
		0.3			V	$V_D = V_{DRM}, R_L = 1\ \text{k}\Omega, T_j = 125\ ^\circ\text{C}$
Peak gate current	I_{GM}		10		A	
Peak reverse gate voltage	V_{RGM}		5		V	
Peak gate power dissipation	P_{GM}		200		W	
Average gate power dissipation	$P_{G(AV)}$		5		W	

Switching

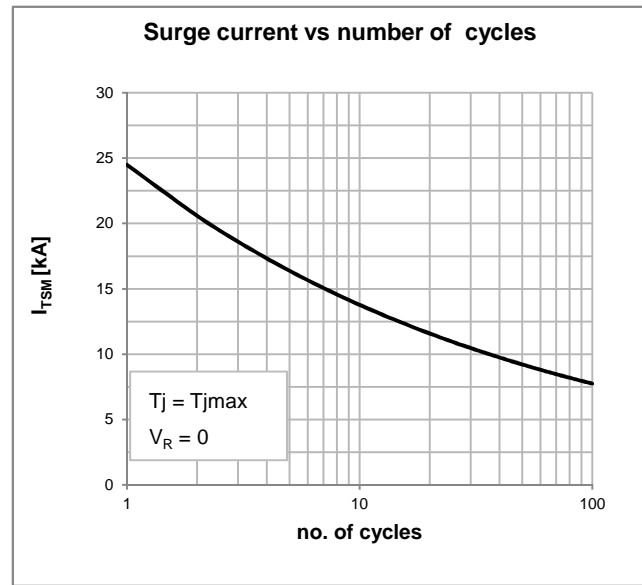
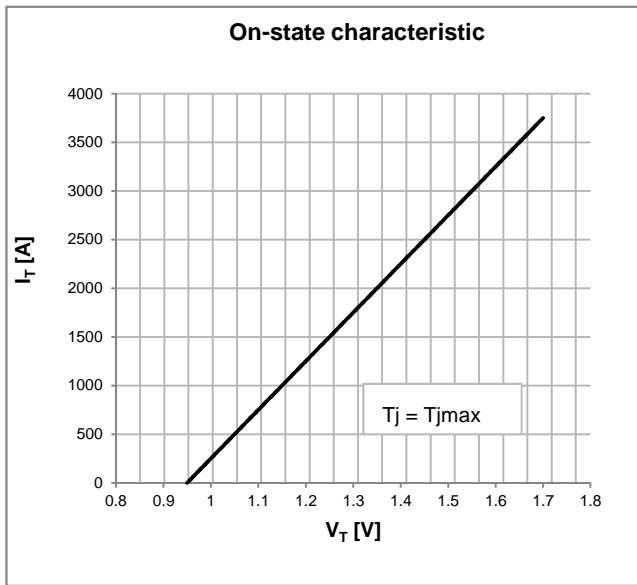
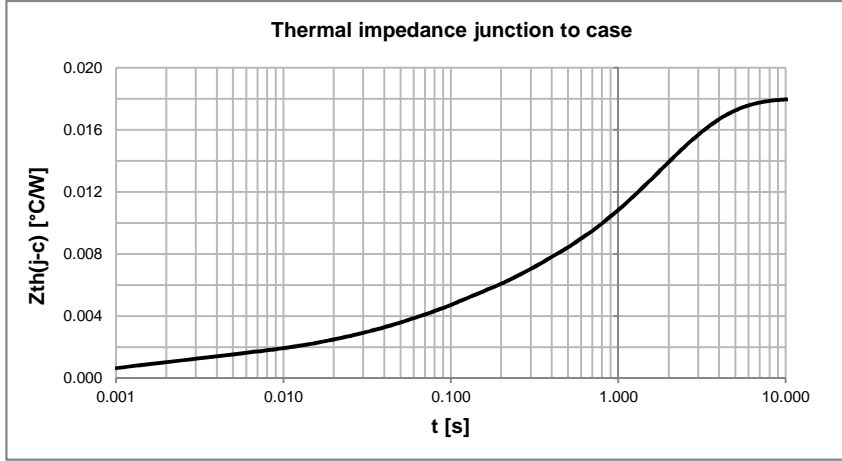
Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Critical rate of rise of on-state current	di/dt		1000		A/ μs	$I_G = 5 \cdot I_{GT}, t_r = 1\ \mu\text{s}, V_{DRM} \leq 1000\text{V}, T_j = T_{jmax}$, non-repetitive
Critical rate of rise of on-state voltage	dv/dt		1000		V/ μs	Linear ramp up to 80% of V_{DRM}
Gate controlled delay time	t_d		1.5	0.7	μs	$I_{TM} = 50\text{ A}, V_D = 67\% V_{DRM}, V_G = 20\text{ V}$ $R_G = 20\ \Omega, t_r = 0.1\ \mu\text{s}, t_p = 20\ \mu\text{s}$
Turn-off time	t_q		400		μs	$I_{TM} = 1000\text{ A}, di/dt = 25\text{ A}/\mu\text{s}, V_R \geq 50\text{ V}$ $dV/dt = 20\text{ V}/\mu\text{s}$ linear to 80% V_{DRM} $V_G = 0\text{ V}; T_j = T_{jmax}$
Reverse recovery charge	Q_{rr}			2700	μC	$I_T = 2000\text{ A}$ $di/dt = 10\text{ A}/\mu\text{s}$
Reverse recovery current	I_{rr}			180	A/ μs	$V_R \geq 100\text{ V}$ $T_j = T_{jmax}$

Thermal and mechanical

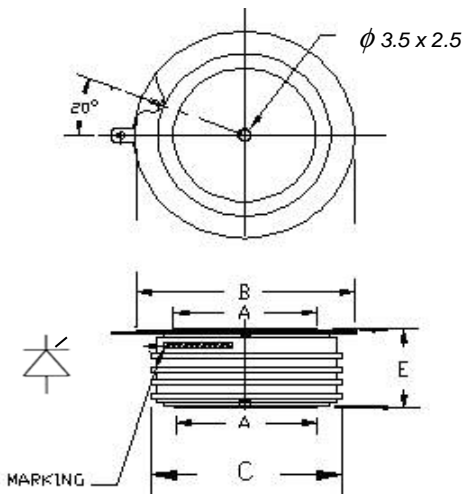
Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Operating temperature	T_j	-40	125		$^\circ\text{C}$	
Storage temperature	T_{stg}	-40	150		$^\circ\text{C}$	
Thermal resistance junction to case	$R_{th(j-c)}$		0.018		$^\circ\text{C}/\text{W}$	Double side cooled, 180° SIN
Thermal resistance case to sink	$R_{th(c-s)}$		0.004		$^\circ\text{C}/\text{W}$	Double side cooled, mounting surfaces smooth, flat and greased
Mounting force	F	20	24		kN	
Weight	W			510	g	

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OUTLINE AND DIMENSIONS



	A	B	C	E
mm	47	74	66	26 ± 0.5

- All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink surfaces with flatness < 0.03 mm and roughness < 2µm