

PST KP5000-14

HIGH POWER PHASE CONTROL THYRISTOR FOR PHASE CONTROL APPLICATIONS

Features :

- Blocking Capability up to 1400 V
- High dV/dt Capability
- All Diffused Structure
- Amplifying Gate Configuration
- Rugged Ceramic Hermetic Package

ELECTRICAL CHARACTERISTICS AND RATINGS

Blocking

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Repetitive peak reverse voltage	V_{RRM}		1400		V	$T_j = -40\text{ °C to }125\text{ °C}$
Repetitive peak off-state voltage	V_{DRM}		1400		V	$T_j = -40\text{ °C to }125\text{ °C}$
Non repetitive peak reverse voltage	V_{RSM}		1500		V	$T_j = -40\text{ °C to }125\text{ °C}$
Repetitive peak reverse current	I_{RRM}		300		mA	$T_j = T_{jmax}, V = V_{RRM}$
Repetitive peak off-state current	I_{DRM}		300		mA	$T_j = T_{jmax}, V = V_{DRM}$

Conducting

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Average value of on-state current	$I_{T(AV)}$		4950		A	50 Hz sine wave, 180° conduction, $T_c = 85\text{ °C}$
RMS value of on-state current	$I_{T(RMS)}$		7772		A	50 Hz sine wave, 180° conduction, $T_c = 85\text{ °C}$
Surge non repetitive current	I_{TSM}		94		kA	50 Hz sine wave Half cycle
I square t	$I^2 t$		44180		kA^2s	$V_R = 0$ $T_j = 125\text{ °C}$
Peak on-state voltage	V_{TM}		1.15		V	On-state current 4800 A, $T_j = T_{jmax}$
Threshold voltage	$V_{T(TO)}$		0.85		V	$T_j = T_{jmax}$
On-state slope resistance	r_T		0.062		$m\Omega$	$T_j = T_{jmax}$
Holding current	I_H			300	mA	$V_D = 24\text{ V}; I_T = 2.5\text{ A}$
Latching current	I_L			1500	mA	$V_D = 24\text{ V}; R_L = 12\ \Omega$

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Triggering

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Gate current	I_{GT}		500		mA	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = -40\ ^\circ\text{C}$
			300		mA	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = 25\ ^\circ\text{C}$
			200		mA	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = 125\ ^\circ\text{C}$
Gate voltage	V_{GT}		5		V	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = -40\ ^\circ\text{C}$
			3		V	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = 0 \div 125\ ^\circ\text{C}$
		0.4			V	$V_D = V_{DRM}; R_L = 10\ \text{k}\Omega; T_j = 125\ ^\circ\text{C}$
Peak gate current	I_{GM}		12		A	
Peak reverse gate voltage	V_{RGM}		5		V	
Peak gate power dissipation	P_{GM}		200		W	
Average gate power dissipation	$P_{G(AV)}$		5		W	

Switching

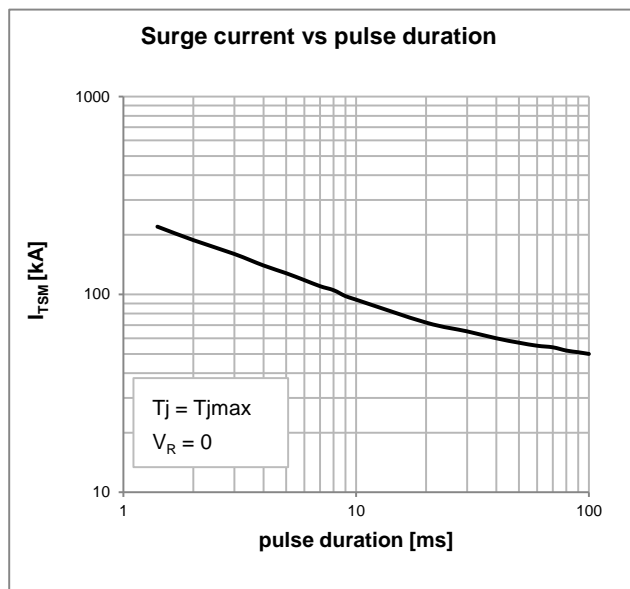
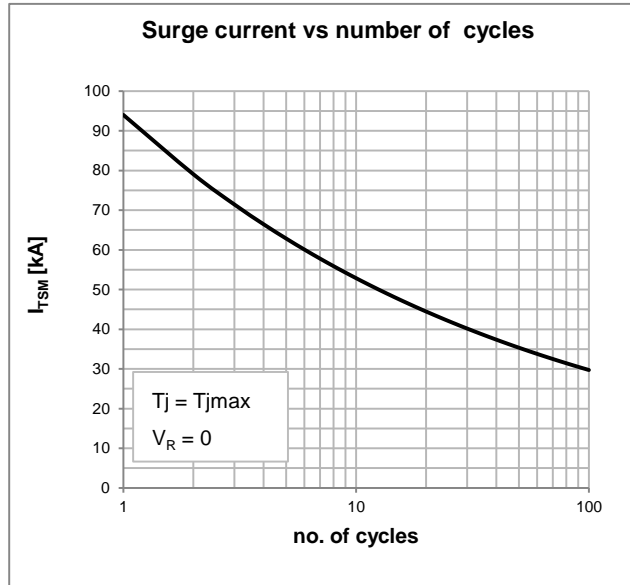
Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Critical rate of rise of on-state current	di/dt		320		A/ μs	Switching from $V_{DRM} \leq 1000\text{ V}$ - repetitive
Critical rate of rise of on-state voltage	dv/dt		1000		V/ μs	Linear ramp up to 80% of V_{DRM}
Gate controlled delay time	t_d		2.5		μs	$I_{TM} = 50\text{ A}; V_D = 1500\text{ V}; V_G = 20\text{ V}$ $R_G = 20\ \Omega; t_r = 0.1\ \mu\text{s}; t_p = 20\ \mu\text{s}$
Turn-off time	t_q		500		μs	$I_{TM} = 2500\text{ A}; di/dt = 25\text{ A}/\mu\text{s}; V_R \geq 50\text{ V}$ $dV/dt = 50\text{ V}/\mu\text{s}$ linear to 80% V_{DRM} $V_G = 0\text{ V}; T_j = 125\ ^\circ\text{C}$
Reverse recovery charge	Q_{rr}			6800	μC	$I_T = 2000\text{ A}$ $di/dt = 20\text{ A}/\mu\text{s}$
Reverse recovery current	I_{rr}			250	A/ μs	$V_R \geq 50\text{ V}$ $T_j = T_{jmax}$

Thermal and mechanical

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Operating temperature	T_j	-40	125		$^\circ\text{C}$	
Storage temperature	T_{stg}	-40	125		$^\circ\text{C}$	
Thermal resistance junction to case	$R_{th(j-c)}$		0.0050		$^\circ\text{C}/\text{W}$	Double side cooled, DC
Thermal resistance case to sink	$R_{th(c-s)}$		0.0010		$^\circ\text{C}/\text{W}$	Double side cooled, mounting surfaces smooth, flat and greased
Mounting force	F	70	90		kN	
Weight	W			2200	g	

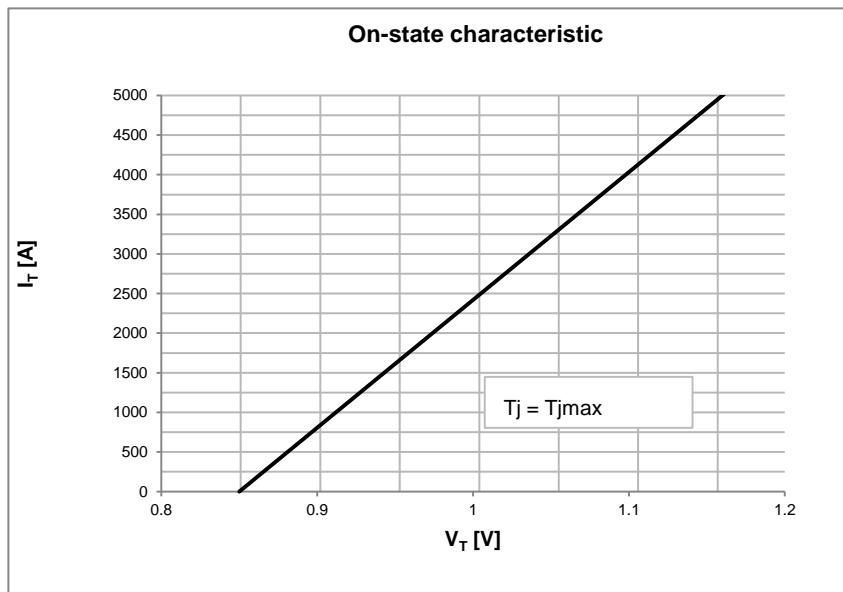
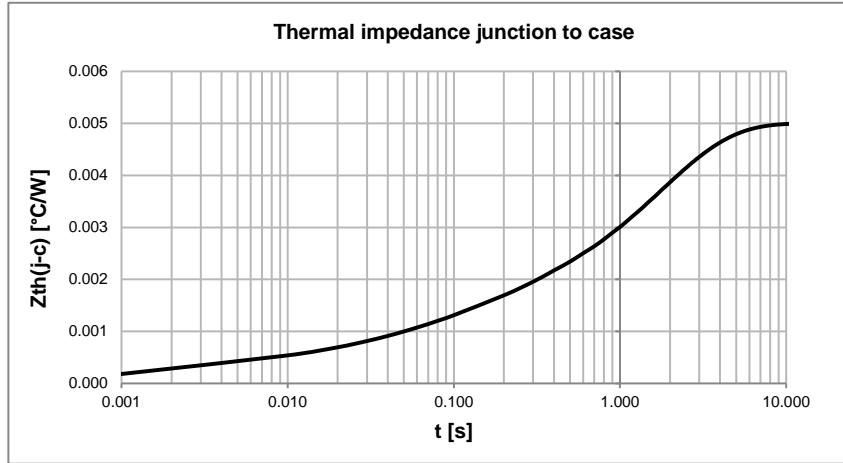
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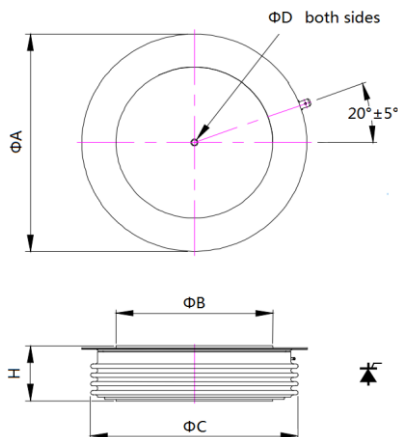


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OUTLINE AND DIMENSIONS



	A	B	C	D	H
mm	150	100	110	3,5 x 3	26+/-1

- All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink surfaces with flatness < 0.03 mm and roughness < 2 μ m