



PST KP1005

HIGH POWER PHASE CONTROL THYRISTOR FOR PHASE CONTROL APPLICATIONS

Features :

- Blocking Capability up to 1800 V
- High dV/dt Capability
- All Diffused Structure
- Amplifying Gate Configuration
- Rugged Ceramic Hermetic Package

ELECTRICAL CHARACTERISTICS AND RATINGS

Blocking

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Repetitive peak reverse voltage	V_{RRM}		1800		V	$T_j = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$
Repetitive peak off-state voltage	V_{DRM}		1800		V	$T_j = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$
Non repetitive peak reverse voltage	V_{RSM}		1900		V	$T_j = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$
Repetitive peak reverse current	I_{RRM}		50		mA	$T_j = T_{jmax}$, $V = V_{RRM}$
Repetitive peak off-state current	I_{DRM}		50		mA	$T_j = T_{jmax}$, $V = V_{DRM}$

Conducting

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Average value of on-state current	$I_{T(AV)}$		1200		A	50 Hz sine wave, 180° conduction, $T_c = 85\text{ }^{\circ}\text{C}$
RMS value of on-state current	$I_{T(RMS)}$		1885		A	50 Hz sine wave, 180° conduction, $T_c = 85\text{ }^{\circ}\text{C}$
Surge non repetitive current	I_{TSM}		23		kA	50 Hz sine wave Half cycle
I square t	$I^2 t$		2645		kA^2s	$V_R = 0$ $T_j = T_{jmax}$
Peak on-state voltage	V_{TM}		1.64		V	On-state current 2900 A, $T_j = T_{jmax}$
Threshold voltage	$V_{T(TO)}$		0.90		V	$T_j = T_{jmax}$
On-state slope resistance	r_T		0.254		$\text{m}\Omega$	$T_j = T_{jmax}$
Holding current	I_H			350	mA	$V_D = 12\text{ V}$; $I_T = 2.5\text{ A}$
Latching current	I_L			800	mA	$V_D = 12\text{ V}$; $R_L = 12\ \Omega$

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Triggering

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Gate current	I_{GT}		350		mA	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = -40\text{ }^\circ\text{C}$
			300		mA	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = 25\text{ }^\circ\text{C}$
			125		mA	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = 125\text{ }^\circ\text{C}$
Gate voltage	V_{GT}		5		V	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = -40\text{ }^\circ\text{C}$
			3.5		V	$V_D = 6\text{ V}, R_L = 3\ \Omega, T_j = 0 \div 125\text{ }^\circ\text{C}$
		0.3			V	$V_D = V_{DRM}, R_L = 1\text{ k}\Omega, T_j = 125\text{ }^\circ\text{C}$
Peak gate current	I_{GM}		10		A	
Peak reverse gate voltage	V_{RGM}		5		V	
Peak gate power dissipation	P_{GM}		150		W	
Average gate power dissipation	$P_{G(AV)}$		3		W	

Switching

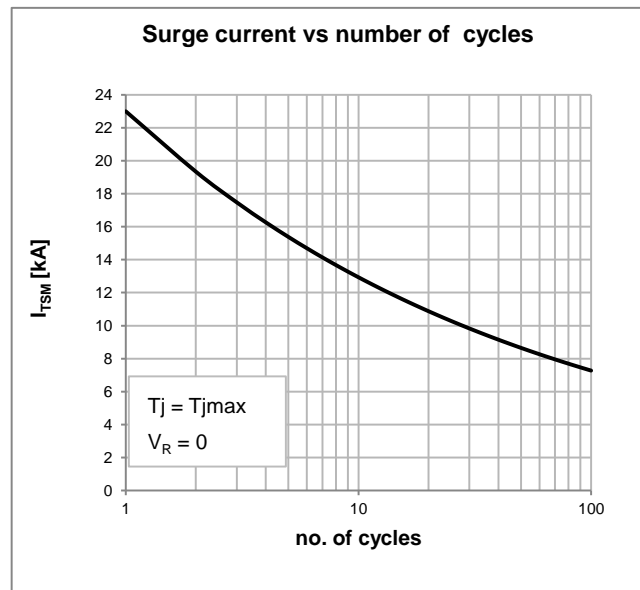
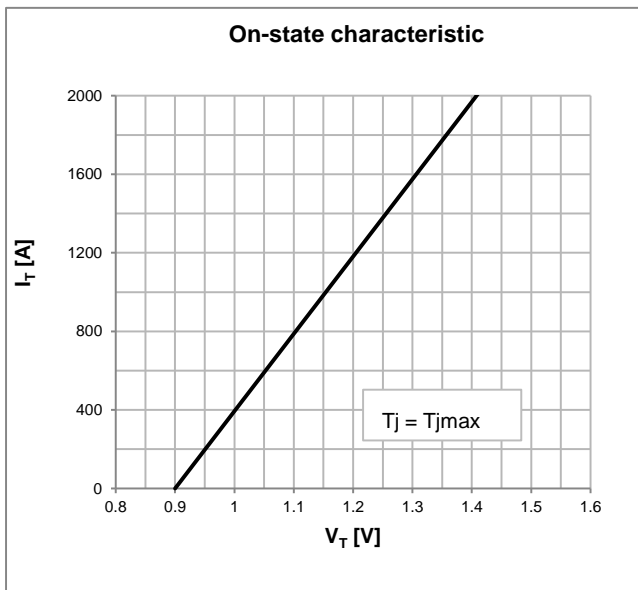
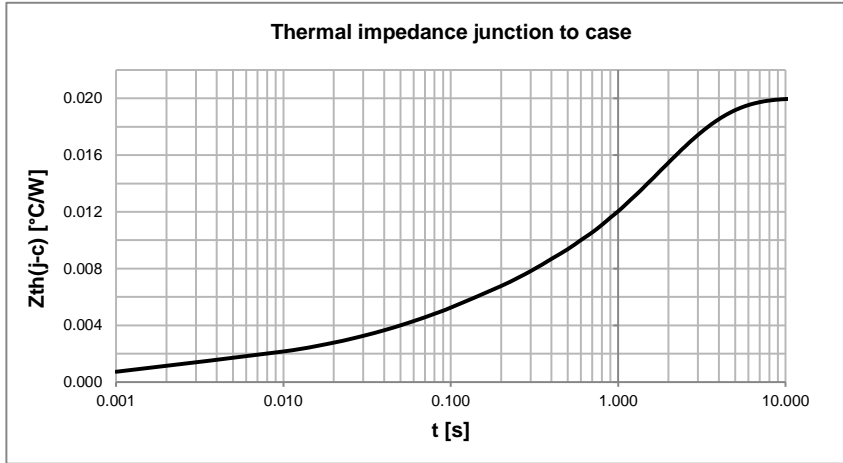
Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Critical rate of rise of on-state current	di/dt		200		A/ μs	$I_G = 5 \cdot I_{GT}, t_r = 1\ \mu\text{s}, V_{DRM} \leq 1500\text{ V}, T_j = T_{jmax}$
Critical rate of rise of on-state voltage	dv/dt		500		V/ μs	Linear ramp up to 75% of V_{DRM}
Gate controlled delay time	t_d			1.5	μs	$I_{TM} = 50\text{ A}, V_D = 67\% V_{DRM}, V_G = 20\text{ V}$ $R_G = 20\ \Omega, t_r = 0.1\ \mu\text{s}, t_p = 20\ \mu\text{s}$
Turn-off time	t_q			250	μs	$I_{TM} = 1100\text{ A}; di/dt = 10\text{ A}/\mu\text{s}; V_R \geq 100\text{ V}$ $dV/dt = 20\text{ V}/\mu\text{s}$ linear to 67% V_{DRM} $V_G = 0\text{ V}; T_j = T_{jmax}$
Reverse recovery charge	Q_{rr}				μC	$I_T = 500\text{ A}$ $di/dt = 20\text{ A}/\mu\text{s}$
Reverse recovery current	I_{rr}				A/ μs	$V_R \geq 50\text{ V}$ $T_j = T_{jmax}$

Thermal and mechanical

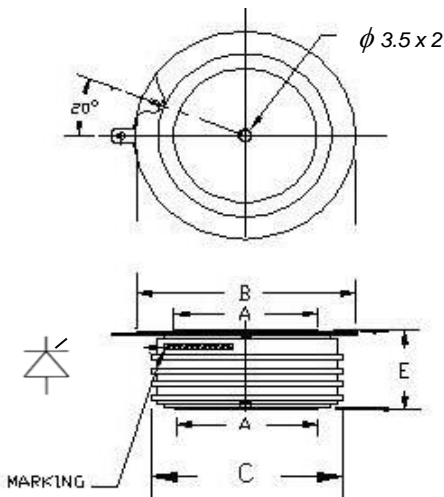
Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Operating temperature	T_j	-40	125		$^\circ\text{C}$	
Storage temperature	T_{stg}	-40	150		$^\circ\text{C}$	
Thermal resistance junction to case	$R_{th(j-c)}$		0.020		$^\circ\text{C}/\text{W}$	Double side cooled, 180° SIN
Thermal resistance case to sink	$R_{th(c-s)}$		0.006		$^\circ\text{C}/\text{W}$	Double side cooled, mounting surfaces smooth, flat and greased
Mounting force	F	20	24		kN	
Weight	W			480	g	

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OUTLINE AND DIMENSIONS



	A	B	C	E
mm	47	75	66	26 ± 0.5

- All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink surfaces with flatness < 0.03 mm and roughness < 2µm