



# PST KP1436

## HIGH POWER PHASE CONTROL THYRISTOR FOR PHASE CONTROL APPLICATIONS

### Features :

- Blocking Capability up to 2800 V
- High dV/dt Capability
- All Diffused Structure
- Amplifying Gate Configuration
- Rugged Ceramic Hermetic Package

### ELECTRICAL CHARACTERISTICS AND RATINGS

#### Blocking

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Repetitive peak reverse voltage	$V_{RRM}$		2800		V	$T_j = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$
Repetitive peak off-state voltage	$V_{DRM}$		2800		V	$T_j = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$
Non repetitive peak reverse voltage	$V_{RSM}$		2900		V	$T_j = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$
Repetitive peak reverse current	$I_{RRM}$		100		mA	$T_j = T_{jmax}$ , $V = V_{RRM}$
Repetitive peak off-state current	$I_{DRM}$		100		mA	$T_j = T_{jmax}$ , $V = V_{DRM}$

#### Conducting

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Average value of on-state current	$I_{T(AV)}$		1436		A	50 Hz sine wave, $180^\circ$ conduction, $T_s = 55\text{ }^\circ\text{C}$
RMS value of on-state current	$I_{T(RMS)}$		2250		A	50 Hz sine wave, $180^\circ$ conduction, $T_s = 55\text{ }^\circ\text{C}$
Surge non repetitive current	$I_{TSM}$		23		kA	50 Hz sine wave Half cycle
I square t	$I^2 t$		2645		$\text{kA}^2\text{s}$	$V_R = 0$ $T_j = T_{jmax}$
Peak on-state voltage	$V_{TM}$		1.89		V	On-state current 2600 A, $T_j = T_{jmax}$
Threshold voltage	$V_{T(TO)}$		1.00		V	$T_j = T_{jmax}$
On-state slope resistance	$r_T$		0.34		m $\Omega$	$T_j = T_{jmax}$
Holding current	$I_H$			400	mA	$V_D = 24\text{ V}$ ; $I_T = 2.5\text{ A}$
Latching current	$I_L$			800	mA	$V_D = 24\text{ V}$ ; $R_L = 12\text{ }\Omega$

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### Triggering

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Gate current	$I_{GT}$		300		mA	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = -40\ ^\circ\text{C}$
			150		mA	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = 25\ ^\circ\text{C}$
			125		mA	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = 125\ ^\circ\text{C}$
Gate voltage	$V_{GT}$		5		V	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = -40\ ^\circ\text{C}$
			3		V	$V_D = 6\text{ V}; R_L = 3\ \Omega; T_j = 0 \div 125\ ^\circ\text{C}$
		0.3			V	$V_D = V_{DRM}; R_L = 10\ \text{k}\Omega; T_j = 125\ ^\circ\text{C}$
Peak gate current	$I_{GM}$		10		A	
Peak reverse gate voltage	$V_{RGM}$		5		V	
Peak gate power dissipation	$P_{GM}$		200		W	
Average gate power dissipation	$P_{G(AV)}$		5		W	

### Switching

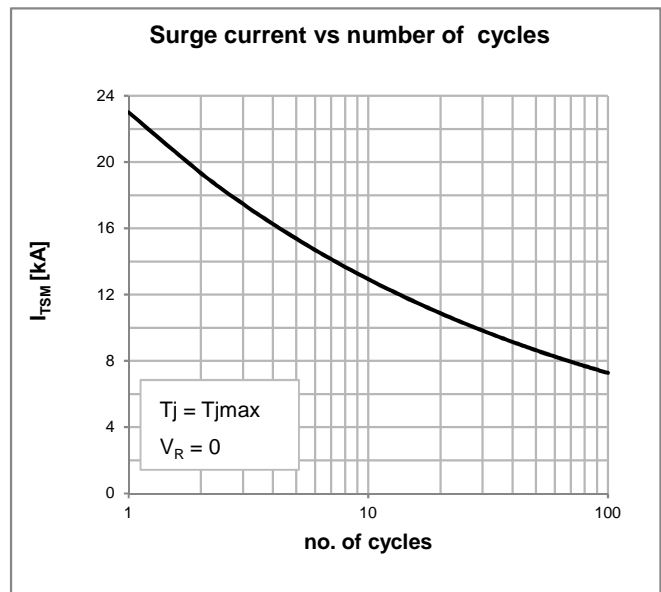
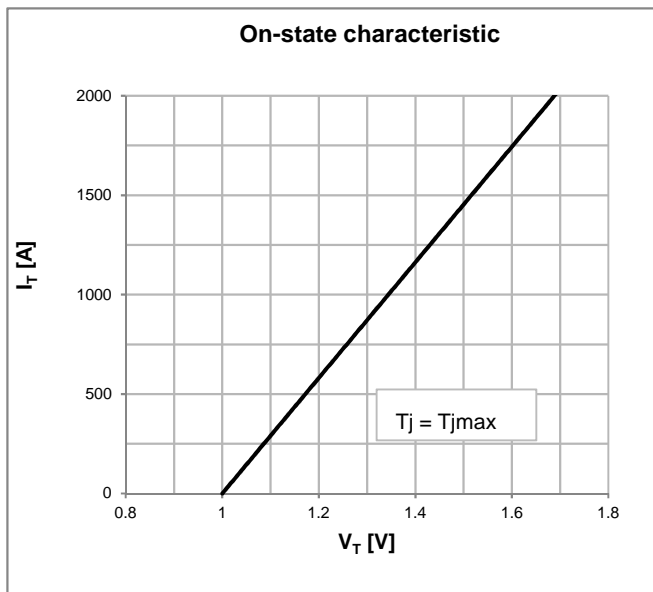
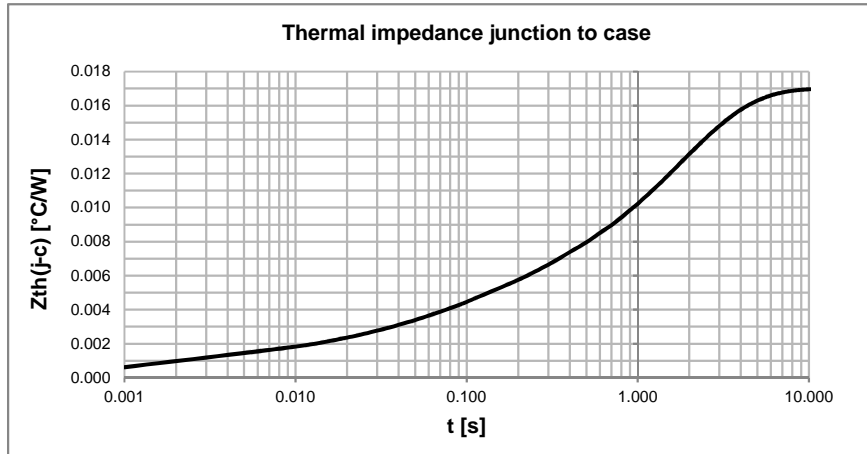
Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Critical rate of rise of on-state current	$di/dt$		400		A/ $\mu\text{s}$	$I_G = 5 \cdot I_{GT}; t_r = 1\ \mu\text{s}; T_j = T_{jmax}$
Critical rate of rise of on-state voltage	$dv/dt$		1000		V/ $\mu\text{s}$	Linear ramp up to 80% of $V_{DRM}$
Gate controlled delay time	$t_d$		1.5	0.7	$\mu\text{s}$	$I_{TM} = 50\text{ A}; V_D = V_{DRM}; V_G = 20\text{ V}$ $R_G = 20\ \Omega; t_r = 0.1\ \mu\text{s}; t_p = 20\ \mu\text{s}$
Turn-off time	$t_q$			250	$\mu\text{s}$	$I_{TM} = 1000\text{ A}; di/dt = 25\text{ A}/\mu\text{s}; V_R \geq 50\text{ V}$ $dV/dt = 20\text{ V}/\mu\text{s}$ linear to 80% $V_{DRM}$ $V_G = 0\text{ V}; T_j = T_{jmax}$
Reverse recovery charge	$Q_{rr}$				$\mu\text{C}$	$I_T = 1000\text{ A}$ $di/dt = 25\text{ A}/\mu\text{s}$
Reverse recovery current	$I_{rr}$				A/ $\mu\text{s}$	$V_R \geq 50\text{ V}$ $T_j = T_{jmax}$

### Thermal and mechanical

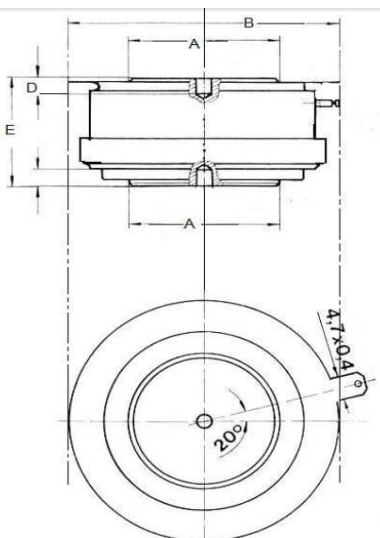
Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Operating temperature	$T_j$	-40	125		$^\circ\text{C}$	
Storage temperature	$T_{stg}$	-40	150		$^\circ\text{C}$	
Thermal resistance junction to case	$R_{th(j-c)}$		0.017		$^\circ\text{C}/\text{W}$	Double side cooled, $180^\circ$ SIN
Thermal resistance case to sink	$R_{th(c-s)}$		0.005		$^\circ\text{C}/\text{W}$	Double side cooled, mounting surfaces smooth, flat and greased
Mounting force	$F$	20	26		kN	
Weight	$W$			475	g	

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### OUTLINE AND DIMENSIONS



	A	B	E
mm	47	75 max	26+/-1
inches	1.85	2.95	1.02



- All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink surfaces with flatness < 0.03 mm and roughness < 2µm