Technical Data

PST KP330

HIGH POWER STUD THYRISTOR
FOR PHASE CONTROL APPLICATIONS

Features :

- Blocking Capability up to 1600 V
- High dV/dt Capability
- Amplifying Gate Configuration
- Ceramic housing

ELECTRICAL CHARACTERISTICS AND RATINGS

Blocking

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Repetitive peak reverse voltage	V_{RRM}		1600		V	Tj = -40 °C to 125 °C
Repetitive peak off-state voltage	V_{DRM}		1600		V	Tj = -40 °C to 125 °C
Non repetitive peak reverse voltage	V_{RSM}		1700		V	Tj = -40 °C to 125 °C
Repetitive peak reverse current	I_{RRM}		50		mA	Tj = Tjmax , V = V_{RRM}
Repetitive peak off-state current	I_{DRM}		50		mA	Tj = Tjmax ,V = V_{DRM}

Conducting

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Average value of on-state current	$I_{T(AV)}$		330		A	50 Hz sine wave,180° conduction, T_c = 75 °C
RMS value of on-state current	$I_{T(RMS)}$		518		A	50 Hz sine wave,180° conduction, T_c = 75 °C
Surge non repetitive current	I_{TSM}		9.0		kA	50 Hz sine wave Half cycle V_R = 0 $T_j = T_{jmax}$
I square t	I^2t		405		kA^2s	
Peak on-state voltage	V_{TM}		1.52		V	On-state current 1000 A, Tj= Tjmax
Threshold voltage	$V_{T(TO)}$		0.89		V	$T_j = T_{jmax}$
On-state slope resistance	r_T		0.63		mΩ	$T_j = T_{jmax}$
Holding current	I_H			600	mA	V_D = 12 V; I_T = 2.5 A
Latching current	I_L			1000	mA	V_D = 12 V; R_L = 12 Ω

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Triggering

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Gate current	I_{GT}		300		mA	V_D = 6 V, R_L = 3 Ω, Tj = - 40 °C
			200		mA	V_D = 6 V, R_L = 3 Ω, Tj = 25 °C
			50		mA	V_D = 6 V, R_L = 3 Ω, Tj = 125 °C
Gate voltage	V_{GT}		4		V	V_D = 6 V, R_L = 3 Ω, Tj = - 40 °C
			3		V	V_D = 6 V, R_L = 3 Ω, Tj = 0 ÷ 125 °C
		0.3			V	V_D = V_{DRM}, R_L = 1 kΩ, Tj = 125 °C
Peak gate current	I_{GM}		3		A	
Peak reverse gate voltage	V_{RGM}		5		V	
Peak gate power dissipation	P_{GM}		10		W	
Average gate power dissipation	$P_{G(AV)}$		2		W	

Switching

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Critical rate of rise of on-state current	**di/dt**		1000		A/µs	$I_G = 8 \cdot I_{GT}$, t_r = 1µs, $V_D \leq$ 80% $V_{DRM.}$ $T_j = T_{jmax}$ - non repetitive -
Critical rate of rise of on-state voltage	**dv/dt**		500		V/µs	Linear ramp up to 80% of V_{DRM}
Gate controlled delay time	t_d			1	µs	I_{TM} = 50 A, V_D = 67% V_{DRM},V_G = 20 V R_G = 20 Ω, t_r = 0.1 µs, t_p = 20 µs
Turn-off time	t_q			120	µs	I_{TM} = 300 A; di/dt = 20 A/µs;$V_R \geq$ 100 V dV/dt = 20 V/µs linear to 67% V_{DRM} V_G = 0 V; $T_j = T_{jmax}$
Reverse recovery charge	Q_{rr}				µC	I_T = 300 A di/dt = 20 A/µs $V_R \geq$ 50 V $T_j = T_{jmax}$
Reverse recovery current	I_{rr}				A/µs	

Thermal and mechanical

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Operating temperature	T_j	-40	125		°C	
Storage temperature	T_{stg}	-40	150		°C	
Thermal resistance junction to case	$R_{th(j-c)}$		0.100		°C/W	180° SIN
Thermal resistance case to sink	$R_{th(c-s)}$		0.030		°C/W	Mounting surfaces smooth, flat and greased
Mounting torque	**M**	44	53		N·m	
Weight	**W**			540	g	

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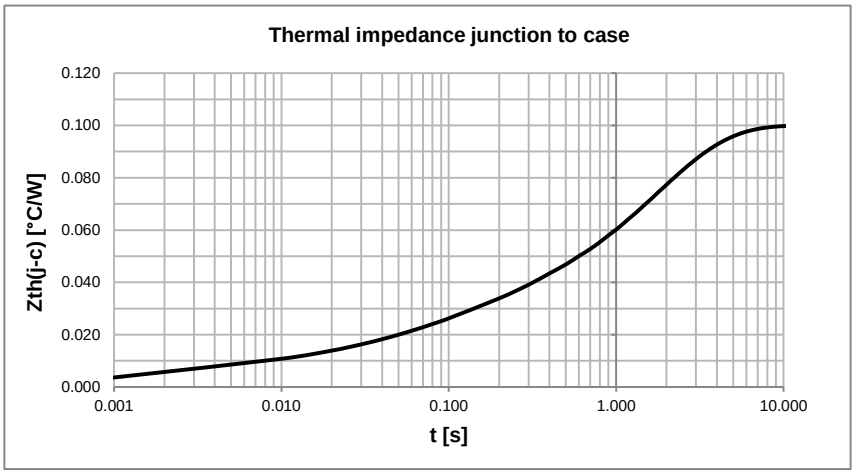

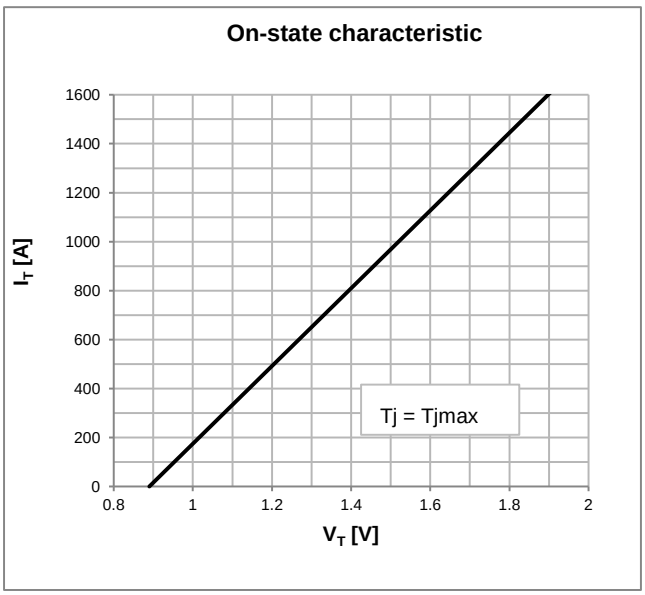

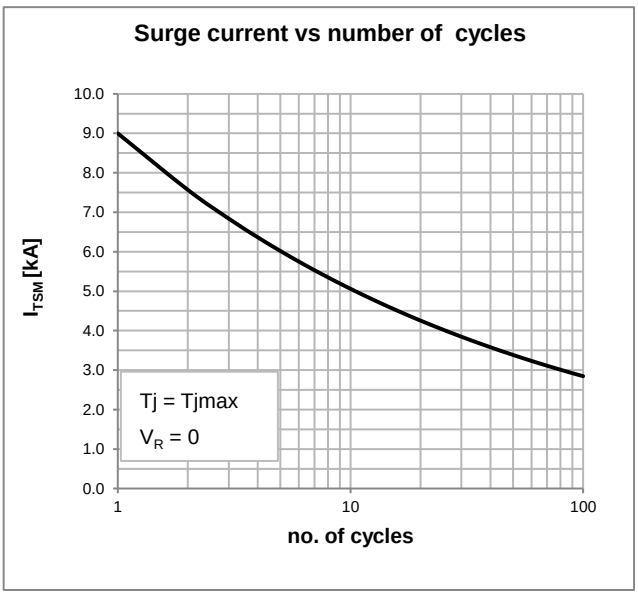

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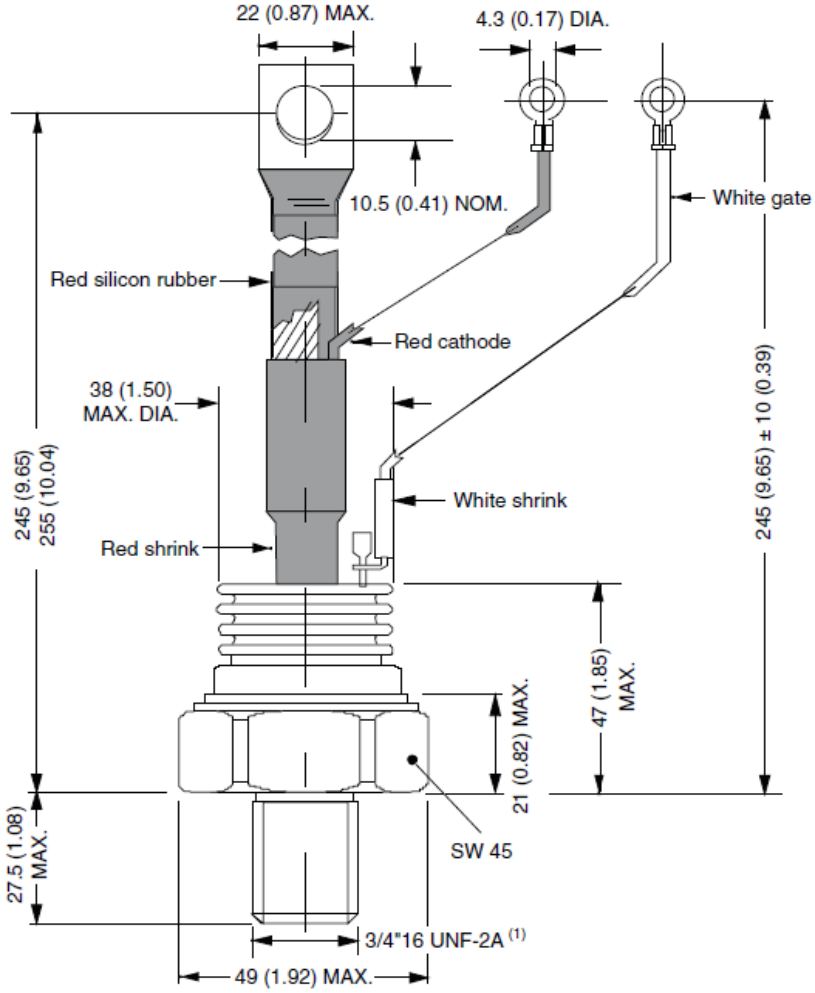
OUTLINE AND DIMENSIONS



dimension in mm (inch)