

PST KP230

HIGH POWER STUD THYRISTOR FOR PHASE CONTROL APPLICATIONS

Features :

- Blocking Capability up to 1600 V
- High dV/dt Capability
- Amplifying Gate Configuration
- Glass-metal seal

ELECTRICAL CHARACTERISTICS AND RATINGS

Blocking

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Repetitive peak reverse voltage	V_{RRM}		1600		V	$T_j = -40^\circ C$ to $125^\circ C$
Repetitive peak off-state voltage	V_{DRM}		1600		V	$T_j = -40^\circ C$ to $125^\circ C$
Non repetitive peak reverse voltage	V_{RSM}		1700		V	$T_j = -40^\circ C$ to $125^\circ C$
Repetitive peak reverse current	I_{RRM}		30		mA	$T_j = T_{jmax}$, $V = V_{RRM}$
Repetitive peak off-state current	I_{DRM}		30		mA	$T_j = T_{jmax}$, $V = V_{DRM}$

Conducting

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Average value of on-state current	$I_{T(AV)}$		230		A	50 Hz sine wave, 180° conduction, $T_c = 85^\circ C$
RMS value of on-state current	$I_{T(RMS)}$		361		A	50 Hz sine wave, 180° conduction, $T_c = 85^\circ C$
Surge non repetitive current	I_{TSM}		5.8		kA	50 Hz sine wave Half cycle
$I^2 t$	$I^2 t$		168		kA ² s	$V_R = 0$ $T_j = T_{jmax}$
Peak on-state voltage	V_{TM}		1.59		V	On-state current 750 A, $T_j = T_{jmax}$
Threshold voltage	$V_{T(TO)}$		0.98		V	$T_j = T_{jmax}$
On-state slope resistance	r_T		0.81		mΩ	$T_j = T_{jmax}$
Holding current	I_H			600	mA	$V_D = 12 V$; $I_T = 2.5 A$
Latching current	I_L			1000	mA	$V_D = 12 V$; $R_L = 12 \Omega$

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Triggering

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Gate current	I_{GT}		200		mA	$V_D = 6 \text{ V}, R_L = 3 \Omega, T_j = -40 \text{ }^\circ\text{C}$
			150		mA	$V_D = 6 \text{ V}, R_L = 3 \Omega, T_j = 25 \text{ }^\circ\text{C}$
			50		mA	$V_D = 6 \text{ V}, R_L = 3 \Omega, T_j = 125 \text{ }^\circ\text{C}$
Gate voltage	V_{GT}		4		V	$V_D = 6 \text{ V}, R_L = 3 \Omega, T_j = -40 \text{ }^\circ\text{C}$
			3		V	$V_D = 6 \text{ V}, R_L = 3 \Omega, T_j = 0 \div 125 \text{ }^\circ\text{C}$
		0.3			V	$V_D = V_{DRM}, R_L = 1 \text{ k}\Omega, T_j = 125 \text{ }^\circ\text{C}$
Peak gate current	I_{GM}		3		A	
Peak reverse gate voltage	V_{RGM}		5		V	
Peak gate power dissipation	P_{GM}		10		W	
Average gate power dissipation	$P_{G(AV)}$		2		W	

Switching

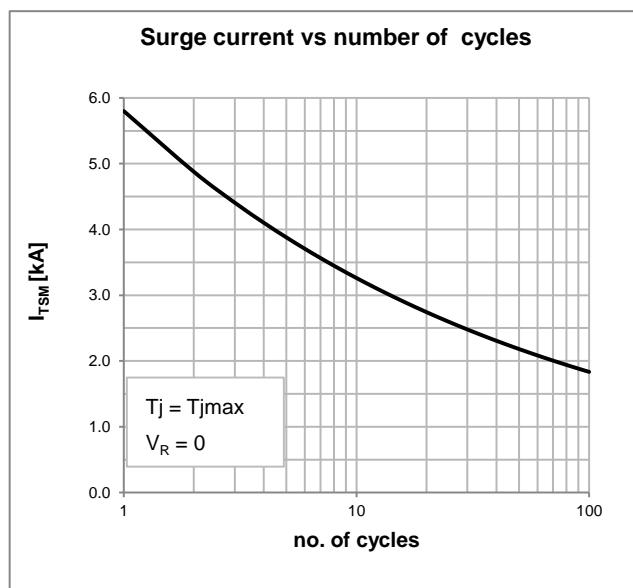
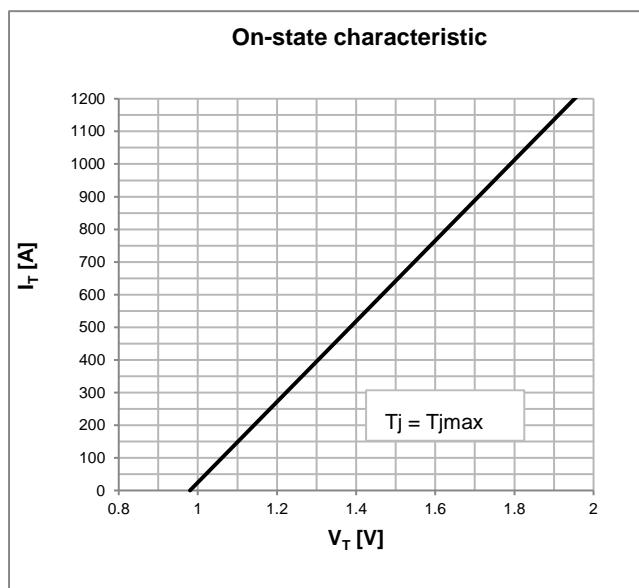
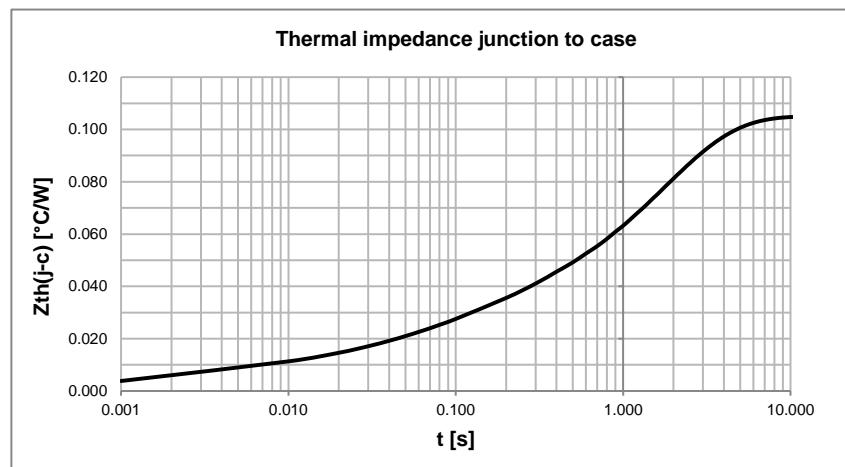
Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Critical rate of rise of on-state current	di/dt		1000		A/ μ s	$I_G = 8 \cdot I_{GT}, t_r = 1 \mu\text{s}, V_D \leq 80\% V_{DRM}, T_j = T_{jmax} - \text{non repetitive}$
Critical rate of rise of on-state voltage	dv/dt		500		V/ μ s	Linear ramp up to 80% of V_{DRM}
Gate controlled delay time	t_d			1	μ s	$I_{TM} = 50 \text{ A}, V_D = 67\% V_{DRM}, V_G = 20 \text{ V}$ $R_G = 20 \Omega, t_r = 0.1 \mu\text{s}, t_p = 20 \mu\text{s}$
Turn-off time	t_q			120	μ s	$I_{TM} = 300 \text{ A}; di/dt = 20 \text{ A}/\mu\text{s}; V_R \geq 100 \text{ V}$ $dV/dt = 20 \text{ V}/\mu\text{s}$ linear to 67% V_{DRM} $V_G = 0 \text{ V}; T_j = T_{jmax}$
Reverse recovery charge	Q_{rr}				μC	$I_T = 300 \text{ A}$ $di/dt = 20 \text{ A}/\mu\text{s}$
Reverse recovery current	I_{rr}				A/ μ s	$V_R \geq 50 \text{ V}$ $T_j = T_{jmax}$

Thermal and mechanical

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Operating temperature	T_j	-40	125		$^\circ\text{C}$	
Storage temperature	T_{stg}	-40	150		$^\circ\text{C}$	
Thermal resistance junction to case	$R_{th(j-c)}$		0.105		$^\circ\text{C}/\text{W}$	180° SIN
Thermal resistance case to sink	$R_{th(c-s)}$		0.040		$^\circ\text{C}/\text{W}$	Mounting surfaces smooth, flat and greased
Mounting torque	M	24.5	31		N·m	
Weight	W			280	g	

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OUTLINE AND DIMENSIONS

